

REMARKS

This Amendment is being filed in response to the final rejection dated April 14, 2005. No new matter is introduced by this amendment. Support for the amendment is found throughout the specification and the accompanying figures, which clearly disclose the active regions and resistor elements extend toward a same direction, each of the resistor elements is formed only on the element isolating insulating film and not formed on the active regions, and the regions including the active regions and the element isolating insulating film are furnished with dummy gate electrode structures. For the following reasons this application should be allowed and the case passed to issue.

Claims 1-22 are pending in this application. Claims 1-3, 5, 11 and 22 are rejected. Claims 4, 6-10, 12, 13, and 21 are objected to. Claims 14-20 are withdrawn pursuant to a restriction requirement. Claims 1, 5, and 22 have been amended.

Initially, it is noted that the status of claims 12 and 13 is not listed on the face of the PTOL-326 Office Action Summary. However, it is noted that on page 7 of the Official Action claims 12 and 13 are objected to as being dependent upon a rejected base claim.

Claim Rejections Under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Raffel et al. (U.S. Patent No. 4,384,299).

Claims 1-3 and 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by Bonser et al. (U.S. Patent No. 6,365,481).

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention, as claimed, and the cited prior art.

An aspect of the invention, per claim 1, is a semiconductor device having a plurality of resistor elements formed on an element isolating insulating film in predetermined regions on a surface of a semiconductor substrate. The semiconductor device comprises active regions proximate to each of the resistor elements. The active regions are formed in the semiconductor substrate and partition the element isolating insulating film between adjacent resistor elements. The active regions and the resistor elements extend toward a same direction. Each of the resistor elements is formed only on the element isolating insulating film, and not formed on the active regions.

The Examiner asserted that Raffel et al. disclose a plurality of resistor elements (100) formed on an element isolating insulating film (114 and 102), and active regions (106) proximate to each of the resistor elements (100), wherein the active regions partition the element isolating insulating film (114). The Examiner included the silicon nitride layer (102) as part of the element isolating insulating film.

Raffel et al. do not anticipate claim 1 because Raffel et al. do not disclose that the each of the resistor elements is formed only on the element isolating insulating film, and not formed on the active regions, as required by claim 1. Raffel et al. disclose the resistor elements (metal strips 100) are formed on the active regions (N-type regions 106).

The Examiner averred that Bonser et al. disclose a semiconductor device comprising a plurality of resistors (30, 32) formed on an element isolating insulating film (16) and active regions (14) proximate to each of the resistor elements. The Examiner maintained that the

recited “is formed only on” in claim 1, when interpreted broadly, could mean “on, but not under.”

Bonser et al. do not anticipate the claimed semiconductor device because Bonser et al. do not disclose that each of the resistor elements is formed only on the element isolating insulating film, and not formed on the active regions, as required by claim 1. Bonser et al. disclose that resistor elements 26, 28 are formed on the active regions 14.

Claims 1, 3, and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by Meyer (U.S. Patent No. 6,285,066). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention, as claimed, and the cited prior art.

An aspect of the present invention, per claim 22, is a semiconductor device having a plurality of resistor elements formed on an element isolating insulating film in predetermined regions on a surface of a semiconductor substrate. The semiconductor device comprises active regions proximate to each of the resistor elements, wherein between portions, formed on the element isolation film, of adjacent resistor elements, the active regions are formed in the semiconductor substrate and partition the element isolating insulating film between adjacent resistor elements. The active regions and the resistor elements extend toward a same direction.

The Examiner alleged that Meyer discloses a semiconductor device having a plurality of resistor elements (138) formed on an element isolating insulating film (136) and active regions (76) partitioning the element isolating insulating film (136) between adjacent resistor elements (138). The Examiner relied on a teaching in Meyer’s background of the invention that field oxides and trenches are used to separate active regions, to conclude that the mesas (76) of Meyer are active regions separated by the isolation trenches.

Meyer does not anticipate the claimed semiconductor device because Meyer does not disclose that the active regions and the resistor elements extend toward a same direction, as required by claims 1 and 22. As illustrated in Fig. 8, the active regions 76 of Meyer form a dot pattern. Meyer does not disclose that the active regions 76 extend toward a same direction as the resistor elements 138.

Claim 5 was rejected under 35 U.S.C. § 102(e) as being anticipated by Moriwaki et al. (U.S. Patent Application Publication No. US 2002/0004270). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention, as claimed, and the cited prior art.

An aspect of the present invention, per claim 5, is a semiconductor device having a plurality of resistor elements formed on an element isolating insulating film in predetermined regions on a surface of a semiconductor substrate. The semiconductor device comprises active regions proximate to each of the resistor elements. The regions including the active regions and the element isolating insulating film are furnished with dummy gate electrodes constituting the same layer as that of the resistor elements.

The Examiner asserted that Moriwaki et al. disclose a semiconductor device having a plurality of resistor elements (103C, 303C) formed on an insulating film (101, 201, 301), and active regions (105, 106, 305, 306) are furnished with dummy gate electrodes (103B and 303B).

Moriwaki et al. do not anticipate the claimed semiconductor device because Moriwaki et al. do not disclose the regions including the active regions and the element isolating insulating film are furnished with dummy gate electrode structures. The Examiner-asserted dummy gate electrodes 103B, 303B of Moriwaki et al. are not formed on the element isolating insulating film, as required by claim 5.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 399, 36 USPQ2d 1101 (Fed. Cir. 1995); *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). Because Raffel et al. and Bosner et al. do not disclose that the each of the resistor elements is formed only on the element isolating insulating film, and not formed on the active regions, as required by claim 1; Meyer does not disclose that the active regions and the resistor elements extend toward a same direction, as required by claims 1 and 22; and Moriwaki et al. do not disclose the regions including the active regions and the element isolating insulating film are furnished with dummy gate electrode structures, as required by claim 5; Raffel et al., Bonser et al., Meyer, and Moriwaki et al. do not anticipate any of claims 1, 5, and 22.

Applicants further submit that Raffel et al., Bonser et al., Meyer, and Moriwaki et al., whether taken alone, or in combination do not suggest the claimed semiconductor devices.

The dependent claims are allowable for at least the same reasons as the independent claims from which they depend and further distinguish the claimed invention.

Allowable Subject Matter

Claims 4, 6-10, 12, 13, and 21 would be allowable if rewritten in independent form and to overcome the indefiniteness rejection. Applicants gratefully acknowledge the indication of allowable subject matter. Applicants note that claim 4 is an independent claim, and thus, should be allowed. As regards claims 6-10, 12, 13, and 21, Applicants do not believe that further

Application No.: 09/960,495

amendment of the claims is necessary because claims 1 and 5 are believed to be allowable, as explained *supra*.

In view of the above amendments and remarks, Applicants submit that this application should be allowed and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Bernard P. Codd

Registration No. 46,429

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BPC:kap
Facsimile: 202.756.8087
Date: October 14, 2005

**Please recognize our Customer No. 20277
as our correspondence address.**